

ANALOG CIRCUIT SIMULATION BY STATE VARIABLE METHOD

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An analog circuit simulation method, based on the state equation approach, is presented. For large time-invariant analog circuits this method automatically formulates the state equations in a symbolic, symbolic-numeric and numeric normal form. According to the proposed circuit analysis method an efficient algorithm that generates the state equations in normal full symbolic, partially symbolic or numeric normal form is described. The SYSEG – SYmbolic State Equation Generation program was improved by the implemented of new routines as: the generation of the state equations in operational form, the reduction of the number of the state equations and the automatic generation of the transfer networks for MIMO circuits. Using the state equations in operational form, the circuit functions in full symbolic, partially symbolic or numeric form are generated.

Keywords: state variables, state equations, symbolic analysis, circuit analysis, circuit functions

1. Introduction

State variable method has the advantage of a remarkable systematization in writing the circuit equations. This is essentially a matrix method and it is the only available method that allows the quality analysis of the analog circuits. The state equation method is used by commercial and professional programs both for linear and nonlinear circuit simulation. This method is wide spread and can be used to solve all the types of circuits including the ones with excess elements.

It uses a minimum number of independent variables (state variables). If these variables are known at the initial time moment $t_0 = 0$, the evolution of the system for $t > t_0$ can be determined. [1-3].

Each complete circuit invariable in time satisfies two basic types of equations: Kirchhoff's laws (KCL and KVL) and the constitutive equations of the circuit elements.

The first order differential equations system, obtained by manipulation of these relations, can be expressed as:

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$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, t), \quad \mathbf{y} = g(\mathbf{x}, t) \quad (1)$$

and represent the state equations of the circuit in normal form, where:

$\mathbf{x} = [x_1, x_2, \dots, x_n]^t$ - is the state vector (x_1, x_2, \dots, x_n - are the circuit state variables, n - is the circuit complexity order);

$\mathbf{y} = [y_1, y_2, \dots, y_p]^t$ - is the output vector (p - is the number of output variables).

For linear and piecewise-linear nonlinear systems the normal matrix form of the state equations is:

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{y} + \mathbf{C}\dot{\mathbf{y}} \quad (2)$$

where:

\mathbf{A} - is the coefficient matrix of the state variables (state matrix) ($n \times n$);

\mathbf{B} - is the coefficient matrix of the input vector ($n \times m$).

\mathbf{C} - is the coefficient matrix of the output vector first order derivatives.

$\mathbf{A}, \mathbf{B}, \mathbf{C}$ matrices contains parameters associated to the nonlinear circuit elements: differential resistances for current controlled nonlinear resistors; differential conductance for voltage controlled nonlinear capacitors; differential inductances for current controlled nonlinear inductors, and differential capacitances for voltage controlled nonlinear capacitors.

A circuit which contains loops made up only by capacitors or/and independent voltage sources or/and voltage controlled sources or cut-sets made up only by inductors or/and independent current sources or/and current controlled sources is known as a circuit with excess elements of the *first order*.

A circuit which contains loops made up only by inductors or/and independent voltage sources or/and voltage controlled sources or cut-sets made up only by capacitors or/and independent current sources or/and current controlled sources is known as a circuit with excess elements of the *second order*, [1, 2, 4].

There are two common methods used to formulate the state equations: the equivalent source method and the topological method of the normal tree.

The equivalent source method for circuits without excess elements consists in replacement of the inductors with ideal independent current sources and of the capacitors with ideal independent voltage sources. For circuits with excess elements an excess inductor is replaced by an ideal independent voltage source with the voltage equal to the inductor voltage. An excess capacitor is replaced by an ideal independent current source with a current equal to the capacitor current.

The topological method of the normal tree can be easily implemented on the computer.

2. The normal tree topological method

In order to generate the state equations a special tree named normal tree is chosen. A normal tree must contain:

- All the independent and all the controlled voltage sources;
- All the controlled branches of the voltage controlled sources;
- All the controlling branches of the current controlling sources;
- As many capacitors as possible (the capacitors that are not in the normal tree are excess elements);
- As many voltage controlled nonlinear resistors;
- As many linear resistors as possible;
- A minimum number of inductors (the inductors that are in the normal tree are excess elements);

A normal tree will not contain any independent and controlled current source or any nonlinear current controlled resistor.

The normal tree will have $n-1$ circuit branches and the corresponding co-tree will have $l-n+1$ circuit branches (n – the number of the circuit nodes; l – the number of the circuit branches). The number of the state variables will be the sum between the capacitors from the normal tree and the inductors from the co-tree.

The co-tree branches are called - *links* and the normal tree branches are called – *normal tree branches (twigs)*. To each normal tree branch (link) it is attached a cut-set (a loop) which contains no other tree branch (link) but links (tree branches). This cut-set (loop) has the orientation identically to the orientation of the attached normal tree branch (attached link), [2].

After choosing all the branches and the associated cut-sets, respectively all the links and the associated loops, a step by step algorithm is followed.

Step 1: Expressing the currents of the current-controlled sources in respect of their controlling variables (according to the definition relations), and taking into account that $i_C = C \cdot dv_C / dt$, the KCL is applied on the cut-sets associated to the tree branch capacitors;

Step 2: Expressing the voltages of the voltage-controlled sources in respect of their controlling variables, and taking into account that: $v_R = R \cdot i_R$, $v_L = L \cdot di_L / dt$, the KVL is applied on the loops associated to the link capacitors;

Step 3: Apply the KVL on the loops associated to the link inductors;

Step 4: Apply the KCL on the cut-sets associated to the tree branch inductors;

Step 5: Write the KCL on the cut-sets associated to the tree branch resistors;

Step 6: Write the KVL on the loops associated to the link resistors;

Step 7: Considering as independent variables the current vectors i_{Rt} , and i_{Rl} , the equations from step 5 and 6 are solved;

Step 8: The symbolic/numeric expressions obtained at the step 7 are introduced into the equations from the step 2 and 4. The equations generated in this way, together with the expressions from the step 7 are introduced into the equations from the steps 1 and 3. Solving these equations in respect of the differentials of the state variables, the state equations in normal symbolic/numeric form are obtained.

3. Description of the SYSEG Program

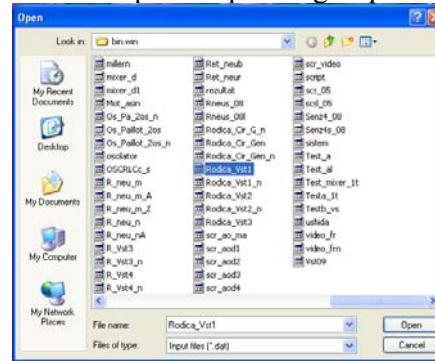
SYSEG – SYmbolic State Equation Generation program, [6], (Fig. 1) was improved by the implemented of new routines as: the generation of the state equations in operational form, the reduction of the number of the state equations and the automatic generation of the transfer networks for MIMO circuits. These circuits may contain both linear and nonlinear resistors, inductors, and capacitors, independent voltage and current sources, and the four types of linear controlled sources. SYSEG program uses the following main window:



Fig. 1. SYSEG program window.

After opening the main window, the following steps are performed:

- Open the circuit input file pressing “Open” button;



- Run the input circuit files by pressing “*Execute Syseg*” button described in Fig.1;
- In order to generate the state equations, the program uses several subroutines shown in Fig.3:

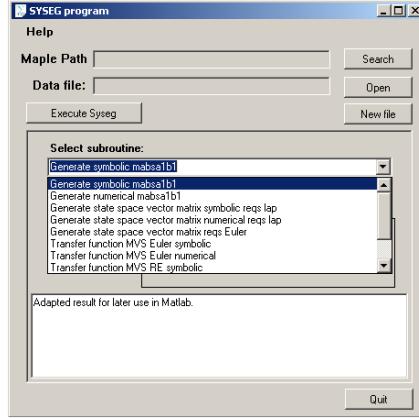


Fig. 3. Program subroutines

- After selecting the subroutine, by pressing the „*Input variables*” button, the excitation quantities will be introduced in the window described in Fig.4;

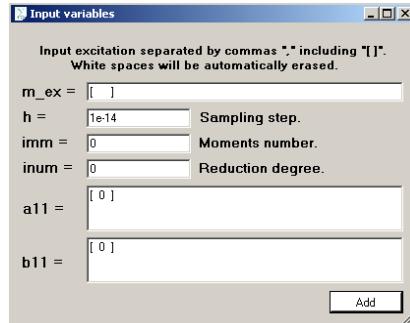


Fig. 4. Input data.

- By pressing „*Input file generation*” button, the input file is generated and the message from Fig. 5 will appear;

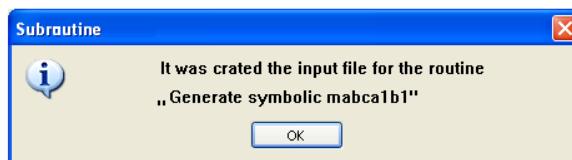


Fig. 5. File generation program window

- Next „Start Maple” button is pressed and the state equations will be obtained by running this file in Maple, [4].

4. Example

A nonlinear circuit with excess elements is presented in Fig. 6. A normal tree that satisfies the requirements presented above is chosen. The circuit in Fig. 6 contains two charge-controlled (q.c.) nonlinear capacitors – C_{du3} and C_{du4} , which have the following characteristics:

$$u_3 = a_{31}q_3 + a_{33}q_3^3 \quad (3)$$

$$u_4 = a_{41}q_4 + a_{43}q_4^3 \quad (4)$$

The circuit has 8 nodes and 10 branches.

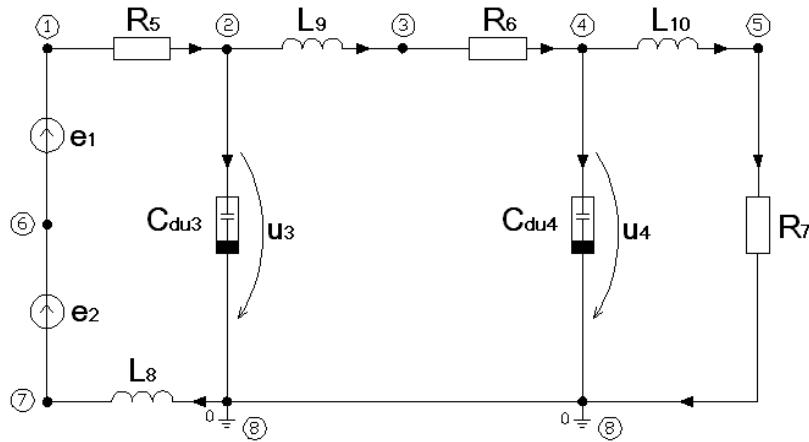


Fig. 6. Diagram of the analyzed nonlinear circuit.

To apply the state variable method, both charge-controlled nonlinear capacitors are substituted by equivalent independent voltage sources. The equivalent circuit is shown in Fig. 7.

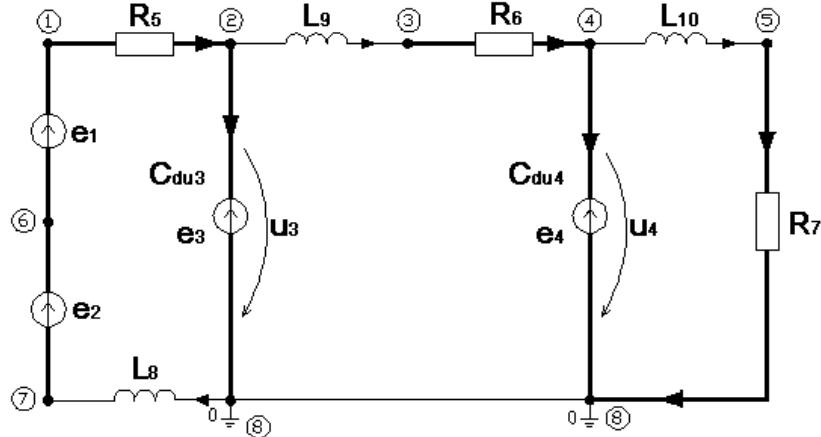


Fig. 7. Diagram of the analyzed circuit – normal tree.

The normal tree (marked by bold lines) and the corresponding co-tree contain the following branches:

$$AN = \{e_1, e_2, e_3, e_4, R_5, R_6, R_7\} \quad (5)$$

$$C_{AN} = \{L_8, L_9, L_{10}\} \quad (6)$$

The number of the state variables results as the sum between the number of capacitors from the normal tree and the number of inductors from the co-tree:
 $n = n_{Ca} + n_{Lc} = 5$.

The state vector \mathbf{x} will be:

$$\mathbf{x} = \begin{bmatrix} q_3 \\ q_4 \\ i_8 \\ i_9 \\ i_{10} \end{bmatrix} \quad (7)$$

Following the above algorithm for the circuit in Fig 7, in which the two nonlinear capacitors were substituted by equivalent independent voltage sources, we get the equations:

$$\dot{q}_3 = i_3 \quad (8)$$

$$\dot{q}_4 = i_4 \quad (9)$$

$$e_3 = u_3 = a_{31}q_3 + a_{33}q_3^3 \quad (10)$$

$$e_4 = u_4 = a_{41}q_4 + a_{43}q_4^3 \quad (11)$$

KVL applied on the loops associated to the link inductors gives:

$$(b_{L_8}): L_8 \frac{di_8}{dt} = -R_5 i_5 + e_1 + e_2 - e_3 \quad (12)$$

$$(b_{L_9}): L_9 \frac{di_9}{dt} = -R_6 i_6 Z + e_3 - e_4 \quad (13)$$

$$(b_{L_{10}}): L_{10} \frac{di_{10}}{dt} = -R_7 i_7 + e_4 \quad (14)$$

KCL applied on the cut-sets associated to the tree branch resistors gives:

$$(\sum R_5): i_5 = i_8 \quad (15)$$

$$(\sum R_6): i_6 = i_9 \quad (16)$$

$$(\sum R_7): i_7 = i_{10} \quad (17)$$

Substituting the equations (15) - (17) into the equations (12) – (14), the symbolic normal-form of the state equations of the circuit in Fig. 7 are obtained:

$$\begin{cases} \frac{di_8}{dt} = -\frac{R_5}{L_8} i_8 + \frac{1}{L_8} e_1 + \frac{1}{L_8} e_2 - \frac{1}{L_8} e_3 \\ \frac{di_9}{dt} = -\frac{R_6}{L_9} i_9 + \frac{1}{L_9} e_3 - \frac{1}{L_9} e_4 \\ \frac{di_{10}}{dt} = -\frac{R_7}{L_{10}} i_{10} + \frac{1}{L_{10}} e_4 \end{cases} \quad (18)$$

From (18) \mathbf{A} , \mathbf{B} , \mathbf{C} matrices will be determined.

$$\mathbf{A} = \begin{bmatrix} -\frac{R_5}{L_8} & 0 & 0 \\ 0 & -\frac{R_6}{L_9} & 0 \\ 0 & 0 & -\frac{R_7}{L_{10}} \end{bmatrix}, \mathbf{B} = \begin{bmatrix} \frac{1}{L_8} & \frac{1}{L_8} & -\frac{1}{L_8} & 0 \\ 0 & 0 & \frac{1}{L_9} & -\frac{1}{L_9} \\ 0 & 0 & 0 & \frac{1}{L_{10}} \end{bmatrix}, \quad (19)$$

$$\mathbf{C} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}.$$

Now we use the Syseg program to analyze the equivalent circuit represented in Fig. 7, which is described by the following input file:

```

10
8
6 1 e1
7 6 e2
8 2 e3
8 4 e4
1 2 R5
3 4 R6
5 8 R7
8 7 L8
2 3 L9
4 5 L10

```

Using *mabsalb1* symbolic generation routine we will obtain the following results:

Number of the state variables

$$n_{stv} = , 3$$

Number of the input (excitation) quantities

$$n_{exq} = , 4$$

Number of the differential input (excitation) quantities

$$n_{dexq} = , 4$$

Number of the output variables

$$n_{outvr} = , 3$$

State vector

$$State_vector = , [IL10, IL8, IL9]$$

Input (excitation) vector y

$$Input_vector y = , [e1, e2, e3, e4]$$

A = a state matrix

$$A = , \begin{bmatrix} -\frac{R7}{L10} & 0 & 0 \\ 0 & -\frac{R5}{L8} & 0 \\ 0 & 0 & -\frac{R6}{L9} \end{bmatrix}$$

B = b matrix of the input (excitation) quantity coefficients

$$B = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L10} \\ \frac{1}{L8} & \frac{1}{L8} & -\frac{1}{L8} & 0 \\ 0 & 0 & \frac{1}{L9} & -\frac{1}{L9} \end{bmatrix}$$

$C = c$ matrix of the differential input (excitation) quantity coefficients

$$C = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

State matrices \mathbf{A} , \mathbf{B} , \mathbf{C} obtained by Syseg program are different from the state matrices (19) because the arrangement of the state variable is different.

Substituting the equations (10), (11) and the equations (15) – (17) into the equations (12) – (14), the symbolic normal-form of the state equations of the circuit in Fig. 6 are obtained:

$$\left\{ \begin{array}{l} \dot{q}_3 = i_8 - i_9 \\ \dot{q}_4 = i_9 - i_{10} \\ \frac{di_8}{dt} = -\frac{R_5}{L_8}i_8 + \frac{e_1}{L_8} + \frac{e_2}{L_8} \\ \frac{di_9}{dt} = -\frac{R_6}{L_9}i_9 + \frac{a_{31}}{L_9}q_3 + \frac{a_{33}}{L_9}q_3^3 - \frac{a_{41}}{L_9}q_4 - \frac{a_{43}}{L_9}q_4^3 \\ \frac{di_{10}}{dt} = -\frac{R_7}{L_{10}}i_{10} + \frac{a_{41}}{L_{10}}q_4 + \frac{a_{43}}{L_{10}}q_4^3 \end{array} \right. \quad (20)$$

The equation system (20) can be written in the following matrix form:

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{A}_1\mathbf{x}^3 + \mathbf{B}\mathbf{y} + \mathbf{C}\dot{\mathbf{y}}, \quad (21)$$

where:

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & -\frac{R_5}{L_8} & 0 & 0 \\ \frac{a_{31}}{L_9} & -\frac{a_{41}}{L_9} & 0 & -\frac{R_6}{L_9} & 0 \\ 0 & \frac{a_{41}}{L_{10}} & 0 & 0 & -\frac{R_7}{L_{10}} \end{bmatrix}, \quad \mathbf{A}_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{a_{33}}{L_9} & -\frac{a_{43}}{L_9} & 0 & 0 & 0 \\ 0 & \frac{a_{43}}{L_{10}} & 0 & 0 & 0 \end{bmatrix},$$

$$\mathbf{B} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{L_8} & \frac{1}{L_8} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad \mathbf{C} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}. \quad (22)$$

If the two charge-controlled nonlinear capacitors are substituted by the two linear capacitors, having the capacitances C_3 and C_4 , and the two ideal independent voltages e_1 and e_2 are substituted by a one independent voltage source denoted by e_i , we can generated the input admittance $Y_{ii}(s) = Y_{7-1,7-1}(s) = \frac{I_{7-1}(s)}{E_i(s)}$, calling the *generate state space vector matrix numerical reqs lap* routine. Using „*Symbolic generation*” (*generate state space vector matrix numerical reqs lap*) routine we obtain the following symbolic expression for the input admittance:

$$\begin{aligned} Y_{ii}(s) := & (1 + s^4 C_3 L_9 C_4 L_{10} + (C_3 R_6 C_4 L_{10} + C_3 L_9 C_4 R_7) s^3 \\ & + (C_3 L_9 + C_3 L_{10} + C_4 L_{10} + C_3 R_6 C_4 R_7) s^2 + (C_3 R_7 + C_4 R_7 + C_3 R_6) s) / (s^5 L_8 C_3 L_9 C_4 L_{10} \\ & + (R_5 C_3 L_9 C_4 L_{10} + L_8 C_3 L_9 C_4 R_7 + L_8 C_3 R_6 C_4 L_{10}) s^4 + (L_9 C_4 L_{10} + L_8 C_4 L_{10} \\ & + R_5 C_3 L_9 C_4 R_7 + L_8 C_3 L_9 + L_8 C_3 L_{10} + R_5 C_3 R_6 C_4 L_{10} + L_8 C_3 R_6 C_4 R_7) s^3 + (R_5 C_3 L_9 \\ & + R_5 C_3 R_6 C_4 R_7 + R_5 C_4 L_{10} + R_5 C_3 L_9 + L_9 C_4 R_7 + R_6 C_4 L_{10} + L_8 C_3 R_6 + L_8 C_4 R_7 \\ & + L_8 C_3 R_7) s^2 + (L_9 + R_5 C_3 R_7 + R_5 C_4 R_7 + L_{10} + R_6 C_4 R_7 + L_8 + R_5 C_3 R_6) s + R_7 + R_5 + R_6) \end{aligned}$$

For the numeric values: $C_3 = C_4 = 0.001$ F, $R_5 = 0.1$ Ω , $R_6 = 0.02$ Ω , $R_7 = 0.02$ Ω , $L_8 = 1$ H, $L_9 = 2.22$ H and $L_{10} = 3.846$ H we obtained the following results:

$$Y_{ii_n} := \frac{1.000000 (s^2 + 0.0084062500 s + 1049.2914) (s^2 + 0.0058029670 s + 111.61991)}{(s + 0.019813217) (s^2 + 0.053611796 s + 1663.3780) (s^2 + 0.040784204 s + 497.53066)}$$

$$\begin{aligned} Poles_Yii_n := & \{ -0.019813217, -0.026805898 - 40.784523 I, -0.026805898 + 40.784523 I, \\ & -0.020392102 - 22.305386 I, -0.020392102 + 22.305386 I \} \end{aligned}$$

$$\begin{aligned} Eigen_Values := & \{ -0.019813217, -0.026805897 - 40.784524 I, -0.026805897 + 40.784524 I, \\ & -0.020392103 - 22.305385 I, -0.020392103 + 22.305385 I \} \end{aligned}$$

$$\begin{aligned} Zerous_Yii_n := & \{ -0.0042031250 - 32.392767 I, -0.0042031250 + 32.392767 I, -0.0029014835 - 10.565032 I, \\ & -0.0029014835 + 10.565032 I \} \end{aligned}$$

We can denote that the poles of the input admittances $Y_{ii}(s) = Y_{7-1,7-1}(s)$ are identically to the eigenvalue values.

6. Conclusions

The state variable method has a high degree of generality and can be applied to any circuit structure, including excess elements. The SYSEG – SYmbolic State Equation Generation program was improved by the implemented of new routines as: the generation of the state equations in operational form, the reduction of the number of the state equations and the automatic generation of the transfer networks for MIMO circuits in symbolic, partially-symbolic, or numeric form. The program was also enhanced by using some new subroutines and a friendly interface.

The circuits to be analyzed may contain both linear and nonlinear elements such as resistors, inductors or capacitors, independent voltage and current sources, and any linear two-ports controlled sources. Starting from a description of the circuit using a netlist file type, the program generates the normal tree, then following a simple algorithm write the circuit equations and finally get the state equations in the desire form. Using an appropriate subroutine, the program can offer also any transfer function in one of the above specified forms.

R E F E R E N C E S

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