

THE BALANCING OF TOTAL LOSSES IN THREE-LEVELS VOLTAGE SOURCE CONVERTERS

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Proiectarea convertoarelor statice de putere trebuie să asigure în orice condiții de funcționare o temperatură a dispozitivelor semiconductoare care să nu depășească limitele admise. Temperatura diferitelor dispozitive semiconductoare depinde de distribuția pierderilor totale și de numărul de întreruptoare în modulele IGBT. În această lucrare se analizează echilibrarea pierderilor totale pentru patru structuri de invertoare cu trei niveluri de tensiune: 3L-Stacked Cells (SC), 3L-Neutral Point Clamped (NPC), 3L-Active NPC (ANPC) și 3L-Stacked NPC (SNPC). Conceptul 3L-SNPC permite dublarea naturală a frecvenței aparente de comutație și conduce la o mai bună echilibrare a pierderilor totale.

Static converters design has to ensure that in all specific operating conditions the junction temperature of power devices does not exceed admitted limits. The temperature of different components depends on the losses distribution and on the number of switches in IGBT modules. This paper investigates the balancing of total losses in four 3L-VSI (Voltage Source Inverters): 3L-Stacked Cells, 3L-Neutral Point Clamped (NPC), 3L-Active NPC and 3L-Stacked NPC. The 3L-Stacked NPC concept allows the natural doubling of the apparent switching frequency and leads to a better balancing of total losses.

Keywords: multilevel converters, conduction losses, switching losses

1. Introduction

Multilevel structures have been studied for over 25 years and they represent an intelligent solution to connect serial switches [1]. The first developed topology has consisted in a serial connection of single-phase inverters with DC separate sources [2]. This structure was followed by a stacked commutation cells concept in order to obtain a multilevel conversion (SC – Stacked Cells) [3-4]. Following the SC structure (Fig.1a), a new multilevel NPC (Neutral Point Clamped) topology was developed [5]. This is the most popular multilevel conversion structure. The 3L-NPC inverters (Fig.1b) are considered a particular way of implementing 3L-SC topology. The role of the middle side in the 3L-SC structure is taken by the inner switches and by the two clamp diodes. Later, another invention [6] introduced the concept of the multilevel converter with

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flying capacitors (FC – Flying Capacitor). In the field of low and moderate frequencies (200 Hz - 1 kHz) the NPC structure is more advantageous than the FC structure because the flying-capacitor size is inversely proportional with the switching frequency. Recently, the 3L-NPC structure performances were improved by developing the 3L-ANPC (Active NPC) converter [7-8] (Fig.1c). In order to obtain a natural doubling of the apparent switching frequency a new conversion structure named 3L-Stacked NPC (Fig.1d) was developed [9].

This paper calculates and compares the losses in power devices between four 3L topologies: 3L-SC, 3L-NPC, 3L-ANPC and 3L-SNPC. The commutation cells are composed by IGBT modules type Mitsubishi CM200DY-24NF, and the clamp diodes are equivalent to the IGBT modules' diodes. The analysis made on the 3L-SC and 3L-NPC topologies proved that the losses in middle side power devices (3L-SC) and the losses in clamp diodes (3L-NPC) increase simultaneously with the reducing of the modulation index. This leads to the increase of the junction temperature in power devices which limits the converters output power, especially at “0” speed operation. The paper shows that 3L-SNPC structure leads to the best balancing of losses in power devices.

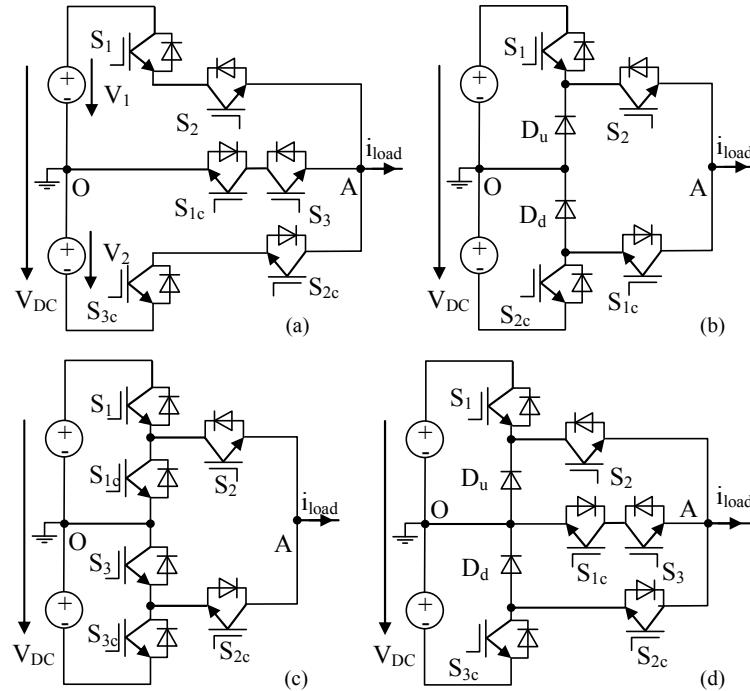


Fig.1. Three-level voltage source inverters: (a) 3L-SC, (b) 3L-NPC, (c) 3L-ANPC, (d) 3L-SNPC.

1. Three-levels voltage source inverters

1.1. Stacked cells structure

The 3L-SC structure is made of six switches disposed on three sides (Fig.1a). Each switch is capable to support a voltage equal to $V_{DC}/2$. The exterior sides are made of two switches serially connected and the middle side is composed by two switches oppositely connected. The switches form three commutation cells (S_1-S_{1c} , S_2-S_{2c} , S_3-S_{3c}) controlled by α_1 , α_2 and α_3 duty cycles. A sinusoidal PWM strategy was used in order to emphasize the constraints applied to 3L-SC converter (Fig.2).

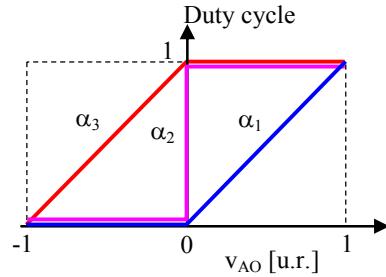


Fig.2. Duty cycles for 3L-SC and 3L-ANPC.

The PWM strategy has four switching states and the output voltage (v_{AO}) has three states: $V_{DC}/2$, 0 and $-V_{DC}/2$ (Table 1). Two switching states (P and N) correspond to direct connection of the load at DC voltage and the other states correspond to "0" voltage level. For $V_{DC}/2$ voltage level (P) the switches S_1 , S_2 and S_3 must be turned on. For $-V_{DC}/2$ level (N) the switches S_{1c} , S_{2c} and S_{3c} must be turned on. The 0^- state is obtained when the S_{1c} , S_{2c} and S_3 are turned on. The 0^+ state is obtained when the S_{1c} , S_2 and S_3 are turned on. The energy conversion is based on two partial uncoupled stages. This represents a disadvantage for the structure. The middle side is common for the both energy conversion stages. This leads to the increase of conduction losses in S_{1c} and S_3 switches, which limits the load current, especially at low modulation index.

Table 1

Output voltage for 3L-SC structure

Output Voltage (v_{AO})	Switching State	Switch Sequence					
		S_1	S_{1c}	S_2	S_{2c}	S_3	S_{3c}
$-V_{DC}/2$	N	0	1	0	1	0	1
0	0^-	0	1	0	1	1	0
	0^+	0	1	1	0	1	0
$V_{DC}/2$	P	1	0	1	0	1	0

1.2. Neutral point clamped structure

The 3L-NPC is the most popular 3L commutation cell (Fig.1b). It is composed by four bidirectional switches and two clamp diodes. Each switch is capable to support a voltage equal to $V_{DC}/2$. The switches form two basic commutation cells: cell-1 (S_1-S_{1c}) and cell-2 (S_2-S_{2c}). These are controlled by α_1 and α_2 duty cycles.

The 3L-NPC structure represents a particular case of the 3L-SC topology. The distinct elements of this circuit are the clamp diodes D_u and D_d . The role of the 3L-SC middle side is taken by the inner switches (S_2 and S_{1c}) and clamp diodes. A sinusoidal PWM strategy was used to analyse the switching states (Fig.3). In comparison with the 3L-SC inverter, the 3L-NPC topology has only three commutation states: P, O and N (Table 2).

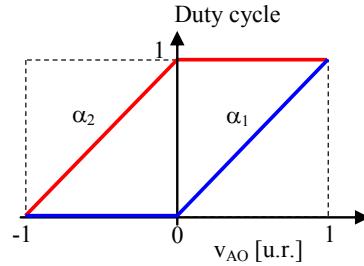


Fig.3. Duty cycles for 3L-NPC topology.

Table 2

Output Voltage (v_{AO})	Switching State	Switch Sequence			
		S_1	S_{1c}	S_2	S_{2c}
$-V_{DC}/2$	N	0	1	0	1
0	O	0	1	1	0
$V_{DC}/2$	P	1	0	1	0

At low reference voltages close to the "0" value the total losses in clamp diodes (D_u and D_d) are bigger than in the other switches and limit the maximum phase current and the switching frequency. Although the two distinct stages are not emphasized like in the 3L-SC case, the two cells commute each on a half cycle.

1.3. Active neutral point clamped structure

The 3L-ANPC structure is obtained by using a parallel connexion of two active switches with the clamp diodes (Fig.1c). This structure is composed by six bidirectional switches disposed on two independent stages. Each switch is capable to support a voltage equal to $V_{DC}/2$. The switches form three commutation cells: cell-1 (S_1-S_{1c}), cell-2 (S_2-S_{2c}) and cell-3 (S_3-S_{3c}). These cells are controlled by α_1 , α_2 and α_3 duty cycles. The control of 3L-ANPC is similar to the one of the 3L-SC structure (Fig.2).

Following the sinusoidal PWM strategy four switching states are obtained: P, N, O^+ and O^- (Table 3). In the case of P and N commutation sequences the paths of the load current through the switches are the same with the 3L-SC and 3L-NPC structures. The “0” voltage level is obtained with two switching states: O^- and O^+ .

Output voltage for 3L-ANPC structure

Output Voltage (v_{A0})	Switching State	Switch Sequence					
		S_1	S_{1c}	S_2	S_{2c}	S_3	S_{3c}
$-V_{DC}/2$	N	0	0	0	1	0	1
0	O^-	0	0	0	1	1	0
	O^+	0	1	1	0	0	0
$V_{DC}/2$	P	1	0	1	0	0	0

1.4. Stacked neutral point clamped structure

The 3L-SNPC structure (Fig.1d) represents a new static conversion concept with three voltage levels [9]. It represents a combination between two well-known conversion concepts: 3L-SC and 3L-NPC. The 3L-SNPC inverter is composed by six bidirectional switches disposed on three sides and two clamp diodes. The exterior sides are made of two switches serially connected (S_1-S_2 and $S_{2c}-S_{3c}$) and the middle side is composed by two switches oppositely connected ($S_{1c}-S_3$). Each switch is capable to support a voltage equal to $V_{DC}/2$. The bidirectional switches are grouped in three basic commutation cells: cell-1 (S_1-S_{1c}), cell-2 (S_2-S_{2c}) and cell-3 (S_3-S_{3c}). These are controlled by α_1 , α_2 and α_3 duty cycles. The clamp diodes D_u and D_d are connected similarly to the 3L-NPC structure.

The 3L-SNPC topology can be controlled with different PWM strategies. In this paper a sinusoidal PWM strategy is presented (Fig.4). It allows the natural doubling of the apparent switching frequency without using the flying capacitor concept. The sinusoidal reference voltage is compared with two carrier waves that

are phase-shifted on the horizontal axis with a half of switching period. In comparison with the other 3L popular commutation cells, the 3L-SNPC cell has six switching states: P, N, O_1^- , O_2^- , O_1^+ and O_2^+ (Table 4).

In order to obtain the switching state P ($V_{DC}/2$), the switches S_1 , S_2 and S_3 must be turned on. The state N ($-V_{DC}/2$) is obtained by turning on the switches S_{1c} , S_{2c} and S_{3c} . In the case of P and N sequences the load current paths through the switches are the same with the other 3L structures studied in the paper. For “0” voltage level, four different control sequences are used: O_1^- , O_2^- , O_1^+ and O_2^+ .

These commutation sequences lead to a natural doubling of the apparent switching frequency similar to the flying-capacitor concept (3L-FC), although the 3L-SNPC inverter does not have flying capacitors. Each switch commutes at the switching frequency f_{sw} , and the output voltage has an apparent switching frequency equal to $2f_{sw}$.

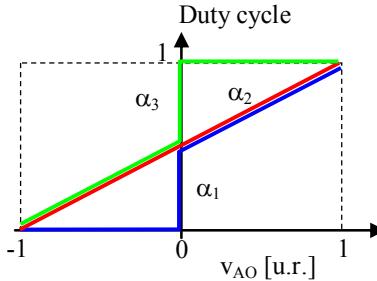


Fig.4. Duty cycles for 3L-SNPC topology.

Table 4

Output voltage for 3L-SNPC structure

Output Voltage (v_{AO})	Switching State	Switch Sequence					
		S_1	S_{1c}	S_2	S_{2c}	S_3	S_{3c}
$-V_{DC}/2$	N	0	1	0	1	0	1
0	O_1^-	0	0	0	1	1	0
	O_2^-	0	1	1	0	0	1
	O_1^+	0	1	1	0	0	0
	O_2^+	1	0	0	1	1	0
$V_{DC}/2$	P	1	0	1	0	1	0

2. Calculus of total losses in power devices

The evolution of temperature in IGBT modules is a direct consequence of the total losses and imposes the maximum power that can be delivered by power switches. The following hypotheses were considered to calculate the losses in power devices:

- all semiconductor devices switch at the same voltage, equal to $V_{DC}/2$;
- the load is considered linear;
- the load current is sinusoidal;
- the current and voltage ripples are neglected;
- the dead times of the IGBT modules are neglected.

The total losses (P_X) are made up of conduction losses (P_{condX}) and switching losses (P_{swX}):

$$P_X = P_{condX} + P_{swX} \quad (1)$$

A) Conduction losses

The conduction losses are obtained as a sum of all conduction losses in transistors (P_{condT}) and diodes (P_{condD}):

$$P_{condX} = P_{condT} + P_{condD} \quad (2)$$

$$P_{condT} = v_{CE0} \cdot I_{avg}^{condT} + r_{dT} \cdot (I_{rms}^{condT})^2 \quad (3)$$

$$P_{condD} = v_{D0} \cdot I_{avg}^{condD} + r_{dD} \cdot (I_{rms}^{condD})^2 \quad (4)$$

where: v_{CE0} , r_{dT} , v_{D0} and r_{dD} – parameters of the transistors and diodes, I_{avg}^{condX} and I_{rms}^{condX} – average and RMS values of the conduction current through X semiconductor.

The expressions for conduction losses depend on the RMS load current (I). The paper presents an example to calculate the conduction losses in T_1 transistor from the S_1 switch (3L-SC, 3L-NPC and 3L-ANPC).

The modulation function for T_1 is sinusoidal:

$$f_{T1}(x) = M \cdot \sin x, \quad x \in [0, \pi] \quad (5)$$

The T_1 transistor is in conduction during $[\theta, \pi]$ interval. As a result, the average and RMS values of the conduction current through T_1 semiconductor can be written:

$$\begin{aligned} I_{avg}^{condT1} &= \frac{1}{2\pi} \int_{\theta}^{\pi} \sqrt{2} \cdot I \cdot \sin(x - \theta) \cdot f_{T1}(x) \cdot dx = \\ &= \frac{I \cdot \sqrt{2} \cdot M}{4 \cdot \pi} \cdot [(\pi - \theta) \cdot \cos \theta + \sin \theta] \end{aligned} \quad (6)$$

$$\begin{aligned}
I_{rms}^{condT1} &= \sqrt{\frac{1}{2\pi} \int_{-\theta}^{\pi} (\sqrt{2} \cdot I \cdot \sin(x - \theta))^2 \cdot f_{T1}(x) \cdot dx} = \\
&= I \cdot \sqrt{\frac{M}{2\pi} \cdot \left[1 + \frac{4}{3} \cdot \cos \theta + \frac{1}{3} \cdot \cos(2 \cdot \theta) \right]}
\end{aligned} \tag{7}$$

For the other switches, the losses are similarly calculated but the modulation functions and the conduction intervals differ from a switch to another for each structure.

B) Switching losses

The IGBTs designers deliver characteristics for the consumed energy at the turning off $E_{off}(I_C)$ and the consumed energy at the turning on $E_{on}(I_C)$. These characteristics depend on the switched voltage (v_{def}) and on the switched current. For an entire switching period, the total energy absorbed by a semiconductor device at v_{def} corresponds to the sum of these energies:

$$E_{vdef}(I_C) = E_{on}(I_C) + E_{off}(I_C) \tag{8}$$

This sum (8) can be approximated with a parabola with A_{swX} , B_{swX} and C_{swX} coefficients:

$$E_{vdef}(I^{swX}) = A_{swX} + B_{swX} \cdot I_{avg}^{swX} + C_{swX} \cdot (I_{rms}^{swX})^2 \tag{9}$$

The following law of proportionality is used to take into consideration the real commutation voltage (v_{sw}) for transistors:

$$E_{vdef}(v_{sw}, I^{swX}) = \frac{v_{sw}}{v_{def}} \cdot E_{vdef}(I^{swX}) \tag{10}$$

For a semiconductor device which switch at f_{sw} on Δ_{sw} interval the switching losses can be written as follows:

$$P_{swX} = f_{sw} \cdot \frac{v_{sw}}{v_{def}} \cdot \left(A_{swX} \cdot \Delta_{sw} + B_{swX} \cdot I_{avg}^{swX} + C_{swX} \cdot (I_{rms}^{swX})^2 \right) \tag{11}$$

where, A_{swX} , B_{swX} , C_{swX} and v_{def} – constants taken from the IGBT's characteristics, Δ_{sw} – ratio between the switching interval and the switching period for semiconductor device, I_{avg}^{swX} and I_{rms}^{swX} – average and RMS values of the switched current through X semiconductor, f_{sw} – switching frequency and v_{sw} – switched voltage.

The expressions for switching currents also depend on the commutation intervals and on the RMS load current (I).

The paper presents an example to calculate the switching losses in T_1 transistor from the S_1 switch (3L-SC, 3L-NPC and 3L-ANPC). This transistor switches on $[\theta, \pi]$ interval. As a result, the average and RMS values of the switching current through T_1 semiconductor can be written as follows:

$$I_{avg}^{swT1} = \frac{1}{2\pi} \int_{\theta}^{\pi} \sqrt{2}I \sin(x - \theta) dx = \frac{I\sqrt{2}}{2\pi} (1 + \cos(\theta)) \quad (12)$$

$$I_{rms}^{swT1} = \sqrt{\frac{1}{2\pi} \int_{\theta}^{\pi} (\sqrt{2}I \sin(x - \theta))^2 \cdot dx} = I \sqrt{\frac{1}{2\pi} \cdot \left(\pi - \theta + \frac{\sin(2\theta)}{2} \right)} \quad (13)$$

This paper compares the losses in power devices between four topologies: 3L-SC, 3L-NPC, 3L-ANPC and 3L-SNPC. The commutation cells are composed by IGBT modules type Mitsubishi CM200DY-24NF, and the clamp diodes are equivalent to the IGBT module diodes.

C) Loss distribution in power devices

The losses in power devices depend on the PWM strategy. In the case of analyzed converters, there are commutation cells that switch at a low frequency and others that switch at a high frequency. The last ones were controlled by sinusoidal duty cycles. The PWM strategies used to control the 3L structures are equivalent and lead to the same output voltages v_{AO} .

The critical points are located at the boundaries of the converter's operating area, being maximum and minimum modulation index (M), at power factor $PF=1$ and $PF=-1$. In these points, the loss distribution presents the biggest lack of balance. All the other operation points are less critical.

Fig.5 shows the loss distribution in switches for the four 3L structures. They were considered two extreme values of modulation index ($M=0.05$ and $M=0.95$) and six values for power factor ($PF=1; 0.86; 0.707; 0.5; 0$ and -1).

The next were observed:

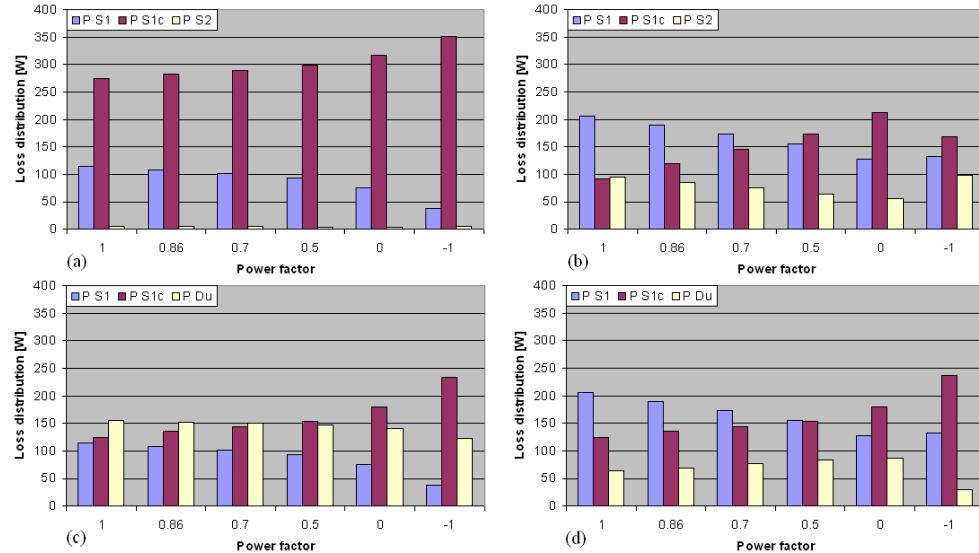
- the middle stage switches (S_{1c} and S_3) from 3L-SC topology limit the maximum phase current at low modulation index;
- in the case of 3L-NPC operation mode, at higher modulation index, total losses in switches are not different from 3L-SC structure;
- for high values of modulation index, the devices that limit the switching frequency and the maximum phase current are the outer ones: for 3L-SC – S_1 and S_{3c} , for 3L-NPC – S_1 and S_{2c} and for 3L ANPC – S_1 and S_{3c} ;

- in the case of low modulation index, the distribution of losses in switches is more uniform in 3L-NPC and 3L-ANPC than in 3L-SC;
- at high modulation index and low power factor ($PF < 0.5$) the losses distribution in switches is more uniform in 3L-ANPC than 3L-NPC, 3L-SC and 3L-SNPC;
- for low modulation index the 3L-SNPC structure allows the best balancing of losses in switches, without taking into account the power factor value;
- for high modulation index and $PF > 0.5$ the 3L-SNPC structure also allows the best balancing of losses in switches.

A better loss-balancing ensures that the operating junction temperatures of all devices do not exceed their limits under all specific operation conditions.

3. Conclusions

In this paper the states and commutation sequences for four 3L topologies (3L-SC, 3L-NPC, 3L-ANPC and 3L-SNPC) have been analyzed. The 3L-NPC structure has 3 switching states, the structures 3L-SC and 3L-ANPC have four switching states, while the 3L-SNPC one has six switching states. As a result, the 3L-SNPC topology has more degrees of freedom than the 3L popular structures and allows the doubling of the apparent switching frequency. This is an important advantage for a better balancing of losses.



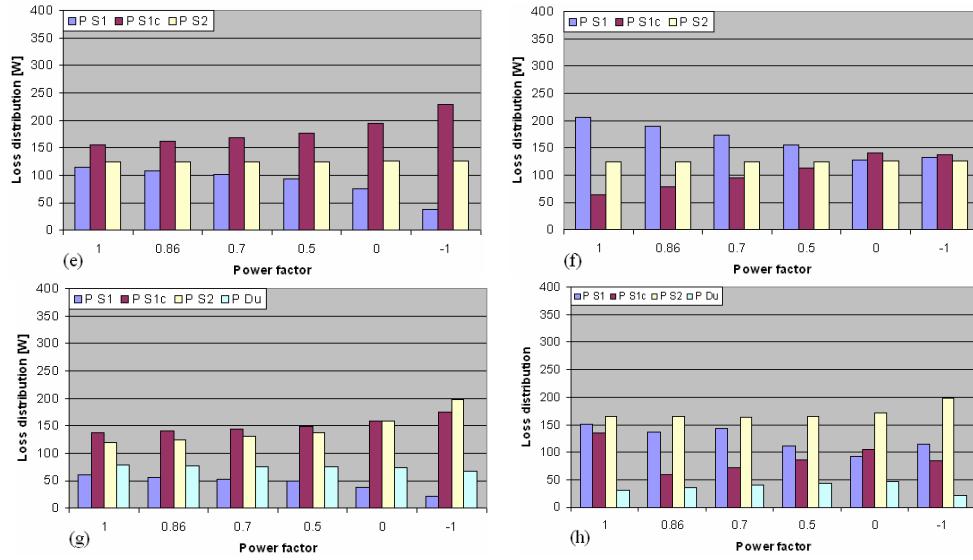


Fig.5. Simulated loss distribution in four 3L topologies (Mitsubishi CM200DY-24NF IGBTs, $I=150A$, $V_{DC}=800V$): (a) 3L-SC ($M=0.05$, $f_{sw}=10kHz$), (b) 3L-SC ($M=0.95$, $f_{sw}=10kHz$), (c) 3L-NPC ($M=0.05$, $f_{sw}=10kHz$), (d) 3L-NPC ($M=0.95$, $f_{sw}=10kHz$), (e) 3L-ANPC ($M=0.05$, $f_{sw}=10kHz$), (f) 3L-ANPC ($M=0.95$, $f_{sw}=10kHz$), (g) 3L-SNPC ($M=0.05$, $f_{sw}=5kHz$), (h) 3L-SNPC ($M=0.95$, $f_{sw}=5kHz$).

An analytic method to calculate the total losses in power devices is also presented and the distribution of losses among the semiconductor devices is investigated. This analysis shows that the total losses in studied converters are not different, but the distribution of losses in switches is unequal and depends on the type of structure, the PWM strategy, the modulation index and the power factor. The total losses in the most stressed switches limit the operation frequency and the maximum phase current of the entire converter.

Compared to the popular 3L topologies (3L-SC, 3L-NPC and 3L-ANPC), the total losses in 3L-SNPC converter are not lower, but a better balancing of losses is obtained.

R E F E R E N C E S

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