

LOW COST AUTOMATED MIXED SIGNAL TEST PLATFORM

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The integrated circuit complexity arises due to usage of modern technologies, client or marketing-imposed specifications, improved functionality or product attractiveness. Each functionality needs to be tested in order to verify datasheet compliance. Testing time and effectiveness need to be improved, due to the close 40% testing costs out of the total product cost. This is achieved by using highly automated mixed signal test platforms and multiple chip test approach.

Present work introduces the prerequisites of a low cost automated mixed signal test platform. It is developed in order to provide test functionality from independent schematic and concept to full product validation. The presented platform is built in order to fill the validation necessities of design and test engineers, by providing adaptability to multiple circuit topologies, easiness in adding test modules and facilitating the connectivity process. The platform is comprised of multiple modules that function alongside with dedicated laboratory equipment.

Keywords: low cost automation, mixed signal testing, embedded test system

1. Introduction

The standardised integrated circuit test system and its additional circuitry necessity is almost a commonness problem. This is one of the prerequisites of any test equipment or method, having the main goal to reduce testing associated expenses, for both software [1] and hardware platforms, especially when dealing with in-house testing procedures [2].

A good part of the overall product cost is allocated to the testing part, design for testability and failure analysis. Therefore, there is the need of continuous improvement and cost reduction of both testing time and test setup. The prerequisites of reducing test costs involve adaptive and low cost test platforms and multiple test chip configurations, thus increasing the test autonomy, by reducing the interface time between test engineer and test setup.

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There are two main directions that involve testing: obtaining a high coverage with low observability [3] or implementing an autonomous integrated test system (self-test) [4].

Product testing is divided on two adjacent directions: circuit functionality analysis contains test methods and principia for the analog, digital modules and interlink between those up mentioned [5] [6] and defect analysis (failure analysis) which comprises defect identification and functionality specific methods for modules and devices [7]. From the functionality standpoint of each component block, the testing proves to be difficult due to the high number of states. The input signal controllability and output observability [5] is obtained using additional circuitry and test equipment for both analogue and digital signals.

Another method regards a summary of system level tests and independent internal block testing, by encapsulating them in individual test-chips. These test-chip will serve as main usage for DUT (device under test) of the test platform. Extended functionality is comprised out of full chip DUTs. The integrated test circuit (test-chip) can contain one or more system blocks, new concepts, trials and circuit variation. Thus, the limited number of pins will impose segregation between the analog and digital signals, functionality and the need of additional serial decoders for configuration. According to functionality, good analog signal division can be obtained using the force-measure behaviour.

The current paper treats the case of low power circuitry, high precision testing, being based on the HP4145/55 [8] [9] semiconductor parameter analyser. This equipment integrates four source-meter channels, 100mA power supplies and two precision voltmeters, and will be the main device used for most analog signal generation and measurement.

In order to gain temperature testing capabilities, the platform will include a Tempronic thermostream system and several additional measurement equipment for analog voltages, currents and frequency. Form the standpoint of forcing and measuring digital response, a PIC microcontroller-based interface will be described. This is comprised out of a 8 bit general purpose 32 outputs PIC microcontroller and a USB to UART converter.

Due to low voltage requirements, the interconnect between the digital signal generation/measurement module and the device under test must be comprised out of a level shifting module. This is designed using low cost operational amplifiers due to the low speed requirements for the digital signals of the platform. A FPGA based digital generation/measurement module is considered for high speed measurement platform enhancement.

For multiplexing the analog test channels, a relay-based multiplexer is used. This is controlled by the same PIC interface. Each multiplexing module is comprised out of 8 double relays and control circuitry. All modules are in the

prototyping stage and have been developed alongside of the system testing requirements.

2. System description

The low cost automated test platform structure is presented in Fig.. 1.

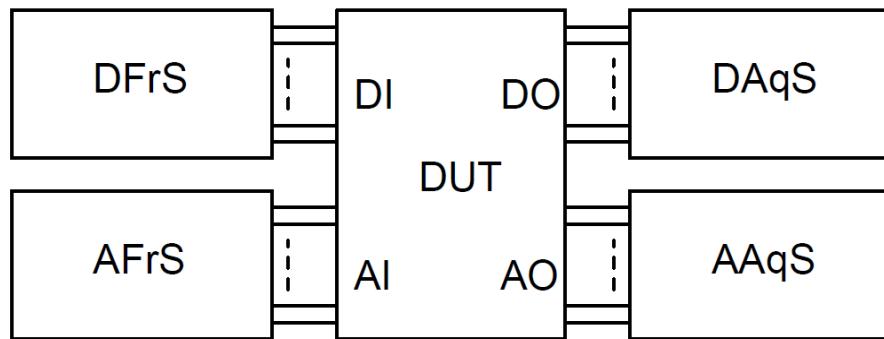


Fig. 1 Low cost automated test platform structure

The system functionality is divided from the stand point of the equipment used for generating and measuring the analog and digital signals, regarding the analog and digital inputs (AI, DI) and outputs (AO, DO) :

- DUT – „Device under test”, is usually an integrated circuit, a testchip enclosing a certain block or concept, or a full product. All tests and platform components have purpose to verify the electrical parameters of the DUT.
- DFrS – „Digital force system”, is the module that controls the digital inputs of the tested circuit; it encloses numerous functions, including the signal level shifting, serial data transmission and synchronization.
- AFrS – „Analog force-measure system” is used for generating analog input signals for the DUT (device under test). This module can enclose numerous equipment for forcing currents and voltages.
- DAqS – „Digital acquisition system” is responsible with recording the digital circuit response; this also encloses a level shifting unit.
- AAqS – „Analog acquisition system” is made up out of analog voltage and current measuring equipment (source meters or precision voltmeters).

Very often testing modules will be combined. For the digital force and acquisition systems will be used a PIC based platform, with 32 input/output ports. This is also capable of controlling relays, in order to multiplex the analog test equipment, adapt the test-bench or provide the prerequisites for the multiple test-chip approach.

3. 8 bit PIC based digital signals force/measure module

The schematic of the digital signal force/acquisition system, with functional blocks depicted, is shown in Fig. 2.

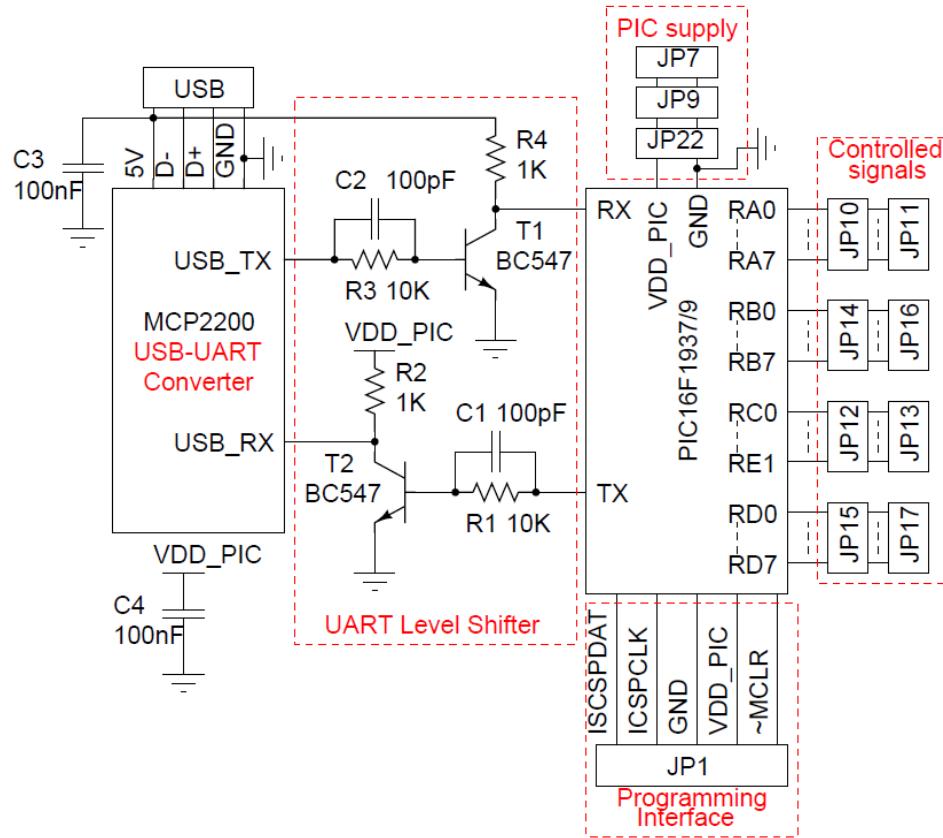


Fig. 2 The schematic of the digital signal force/acquisition system

The system is based on an 8-bit microcontroller, PIC16F1937 / 9 [10] and a USB-UART converter. It has 32 configurable pins via the test program to be digital input or output. Communication with the microcontroller is performed via the UART serial interface, using the USB-UART MCP2200 [11] converter.

The USB-UART converter is supplied using the USB interface and the microcontroller uses an external supply. External connectivity is gained using JP1 connector for the PicKit 2 or 3 programming header and JP7/9/22 for powering the module. The connectivity between the microcontroller ports and device under test is provided using pinheads with two rows, for each 8 bit: JP10/11 for port A, JP14/16 for port B, JP15/17 for port D and JP12/13 for two bits for E and 6 port C. Port C cannot be used entirely due to the UART proprietary connectivity of RC6 and RC7 UART.

For the UART interface, transistors T1 and T2, resistors R1-R4 and capacitors C1, C2 form an inverting level shifting circuit for the UART TX and RX signals. Initially this was used in the absence of the dedicated level shifter circuit, by powering the microcontroller from the same voltage supply as the device under test. This is no longer used due to the under power on reset voltage requirements for the power supply. The level shifter circuit, which will also be presented in this paper, is no longer dependent on the minimum DUT supply voltage, thus keeping the digital signals force/measurement module supply at 5V.

The printed circuit board for the digital signal force/acquisition system is depicted in Fig. 3. This is designed using two layers, most of the interconnects being on the bottom side. By limiting top layer connectivity, the prototyping process is enhanced. Limiting the overall printed circuit board area, cost effective components and low assembly time, resides in a very low cost module, which is easily reproduced.

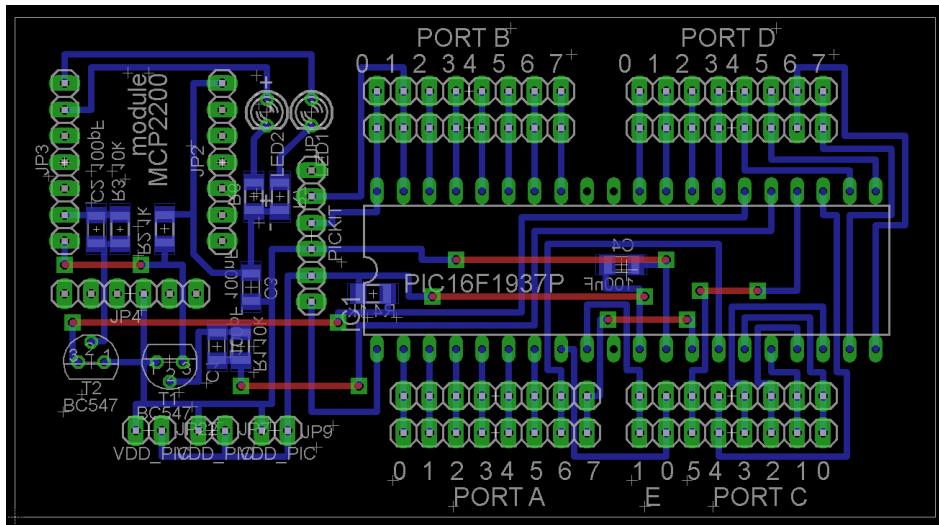


Fig. 3 The printed circuit board of the digital signal force/acquisition system

4. Low cost level shifters

Using off-the-shelf level shifters would increase the total cost of the test platform. For example, the 74LVC8T595PWJ [12] product from Nexperia has the cost of about 1 euro a piece, compared with the MCP601 which has one fourth of the price.

Regarding the supply voltage limitation, the Nexperia has the lowest supply voltage of about 1V. As for the level shifters based on difference circuits, the minimum supply voltage limitation no longer exists. This ensures that the platform is ready for higher circuit scaling that imply much lower supply voltages.

From the standpoint of printed circuit board and additional components, the integrated level shifters carry additional costs, as for the OPAMP based one, the additional components are limited to some resistors and noise decoupling capacitors. The drawback of using low cost OPAMP based level shifters is that they provide a lower speed solution compared with the integrated ones. In Fig. 4, the low cost level shifting circuit for the DFrS is depicted.

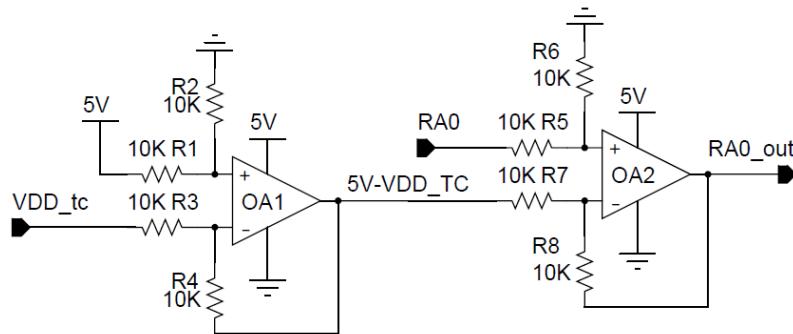


Fig. 4 The low cost level shifting circuit for the DFrS channels

The circuit uses two differentiating circuits. The first one is comprised out of OA1 operational amplifier and R1-R4 resistors. This circuit is used for generating a reference voltage and it computes the difference between the 5V supply voltage of the digital signal force/acquisition system and the test-chip supply voltage, VDD_tc, with the range between 0-3.3V.

OA2 operational amplifier computes the difference between the voltage of one of the microcontroller ports (RA0, which has the voltage range between 0-5V) and the up mentioned reference voltage. OA2 circuit will be multiplied in order to match the number of ports used, by maintaining groups of 8 bits. In this case, RA0_out is the logic signal that will control the DUT (device under test), that has the voltage range adapted to the supply voltage of the tested circuit (VDD_tc).

Considering R1:R8 equal resistors, the output of OA1 and OA2 is rewritten in equation 1 and 2. The circuit in Fig. 2 adapts the 0-5V to 0-VDD_tc voltage domain.

$$V_{out_OA1} = 5V - VDD_tc \quad (1)$$

$$V_{out_OA2} = V_{RA0} - (5V - VDD_tc) \quad (2)$$

From equations 1 and 2 it is clear that the output voltage of the level shifting circuit will track the one of the test-chip, ensuring functionality even for low supply voltages.

For level shifting the DAqS side, there can be used a simple comparator with a 1:2 voltage divider as reference, connected to the test-chip supply voltage

(VDD_tc). OUT_tc is one of the DUT outputs and RA0_in will have the voltage levels adapted to the microcontroller supply. This method ensures that no matter the device under test supply voltage, the output will be in the 0-5V range of the microcontroller. This circuit is depicted in Fig. 5.

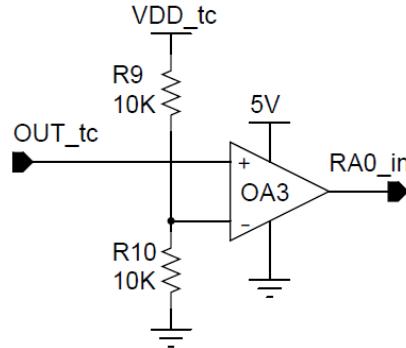


Fig. 5 Level shifter circuit used in DAqS

The complete printed circuit board for 8 bit port using the circuit presented in Fig. 4, is depicted in Fig. 6. It used 9 SOT23-5 MCP601 operational amplifiers, 8 for each bit of the port and one for generating the reference voltage. On the left side of the printed circuit board is the supply voltage connector for both the 5V microcontroller and test-chip supply. Due to the fact that most of the components are surface mount, the PCB size is half of the lowest price unit, in terms of fabrication. Using off the shelf inexpensive components, adds to the low cost prerequisites of the presented platform.

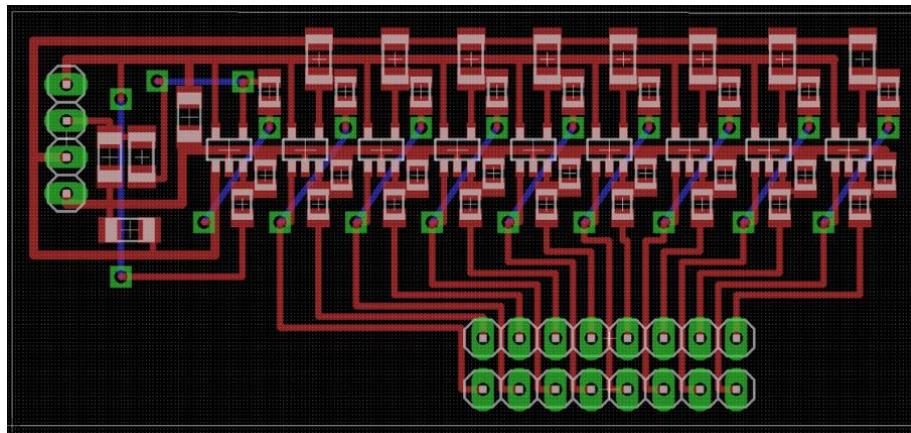


Fig. 6 The low cost level shifting circuit for the DFrS channels printed circuit board

5. Analog signals multiplexing

The number of analog force/measure testing equipment is reduced due to its high cost. Opposed to the digital test equipment, the analog has a limited number of channels, therefore analog multiplexing circuitry is necessary.

A variant for the printed circuit board for the analog multiplexing circuit is depicted in Fig. 7. This is comprised out of 8 double relays, complete with the controlling circuitry.

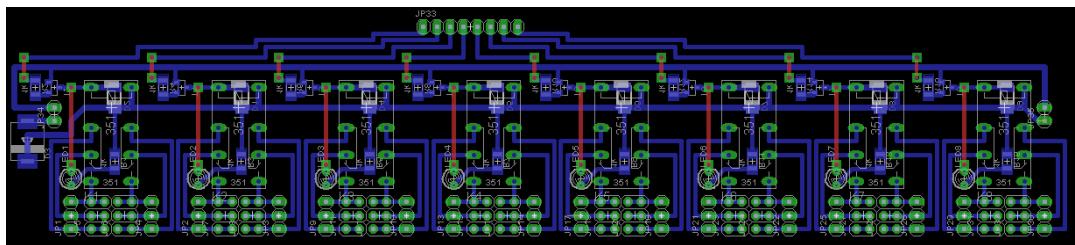


Fig. 7 Relay based analog multiplexer printed circuit board

The supply voltage is the same as the microcontroller in the digital signal force/acquisition system. Over time, there were assembled six 8 relay modules, depending on the evolution of both test program, tested circuits and platform. The 5 volt logic can be controlled by one of the microcontroller ports, assuring the digital signal force/acquisition system of multifunction prerequisites. For example, certain bits can be used as digital data input or output and others to control the analog multiplexing, all provided by one module.

The analog multiplexing modules provide connectivity for both standard 0.75mm pinhead connectors and proprietary HP4145/55 1mm connectors. This ensures flexibility in building test-benches, in both mono-chip and multi-chip test approaches.

6. Conclusions

The presented platform in this paper encloses the following modules: digital signal force/acquisition system, level shifting modules and analog multiplexing features for both mono-chip and multi-chip test approaches. Using Perl based scripting instead of a dedicated software as Labview [13] and a low cost 8-bit microcontroller controlled by Perl scripts, has a cost minimizing effect from both software and hardware.

Automated measurement microcontroller-based platforms prove to be a cost optimized solution for a high variety of applications [14], due to their versatility in usage. The platform encloses the following features:

- Adaptability – the multitude of test setups and interchangeable configurations that can be achieved fits most of the individual block and concept testing prerequisites.
- Low cost – most of the components are general use and interchangeable
- Future development capability – the modules already designed are interconnected using wires and can be upgraded without interfering with the main control system; in order to accomplish future functionality, new modules can be added using same control interface
- Low user maintenance – most components are using sockets in order to provide easy debugging and maintenance; pinheads are used, so that the eventual connectivity failures can be fixed by using a new set of wires
- Low user handling – after the test setup has been developed, the platform can run autonomous for tens of thousands of measurements, providing continuous operation.

The circuits for level shifting are using MCP601 [15] operational amplifiers, in SOT23-5 package. This provides high covering of the printed circuit board area. There are four 8 channel modules, one for each 8 bit port.

Comparison between a similar solution for the digital force/acquisition system, NI USB-6008/9 [16], and an analog multiplexing system, Keysight 34970A [17], is provided in table 1.

Table 1

Digital force/acquisition system and analog multiplexer comparison

Digital force/acquisition system		
	Digital force/acquisition system + Level shifters	National Instruments USB-6009 [16]
Digital I/O	32	13
Digital I/O config.	manual	automatic
Analog inputs	0	8
Analog outputs	0	2
Control	Perl scripts (Free)	LabView (Licence req.)
Price	~1x	~10x
Analog multiplexing system		
	Digital force/acquisition system +4 relay boards	Keysight 34970A + 34901A [17]
No. of channels (max)	4x8 double	3x20
Max. Current/Voltage	2A/250V	1A/300V
2wire/4wire	Yes	Yes
Speed ch/sec	10	60
Connectivity	header, 3 pairs/channel	terminal blocks
Price	~1x	~20x

For most of the items compared, the new platform provides improved functionality at low cost.

Future development includes multichip testing modules, high frequency and voltage signal generation/measurement enhancement and automatic configuration for the digital I/O ports. This will make the platform suitable for characterization of a large circuit domain, including oscillator frequency and duty cycle [18], phase locked loops and converters.

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