

SIGNAL PROCESSING FOR INTEGRATED HALL EFFECT SENSORS USING SWITCHED CAPACITOR CIRCUITS

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În această lucrare se vor prezenta noi tehnici de prelucrare a semnalelor electrice generate de traductori magnetici Hall folosind circuite cu capacități comutate, comparații cu tehnicile actuale de prelucrare actuale și performanțele obținute prin utilizarea fiecăreia dintre ele, împreună cu recomandări privind alegerea lanțului de semnal optim.

This paper presents new signal processing techniques for Hall effect transducers, using switched capacitor circuits, along with comparisons to the presents signal processing techniques and their performances and recommendations for choosing the right signal path architecture and achieving a good compromise between performance and used resources.

Keywords: Hall effect, transducer, signal path, sampling, temperature compensation, offset, noise, sensitivity, switched capacitor

1. Introduction

Hall effect sensors have been used for some time in application where presence detection over short distances is required, as a replacement for mechanical transducers. This has yielded improvements in reliability and manufacturing cost. The integration of the Hall transducer along with the signal conditioning circuit has improved overall performance and at the same time reduced the application cost.

The implementation of a Hall transducer in an integrated technology itself is not a difficult process. Any resistive diffusion can be used as a primitive transducer, in a bipolar, CMOS or BiCMOS process. The transducer requires four contacts, two for biasing and two for sensing.

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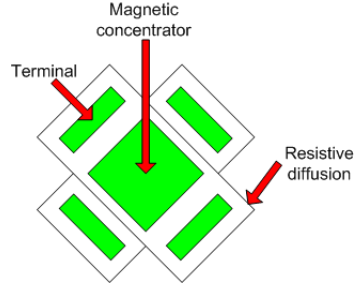


Fig. 1. Symmetrical Hall plate layout

Biasing the transducer can be done in two ways: either voltage or current. While voltage biasing is fairly easy to be done, using a voltage regulator which supplies the whole chip, using current biasing the performance of the sensor can be greatly improved by compensating the sensitivity variation over the operating temperature range.

Over the years, several signal processing techniques have been developed in order to improve the accuracy of the output voltage reading of the Hall transducer.

2. Nonlinear effects in Hall transducers

The ideal Hall effect transducer generates an output voltage that is directly proportional to the magnetic field applied and the intensity of the current which passes through it

$$V = \frac{R_H}{t} IB_{\perp} \quad (1)$$

where V is the Hall voltage, R_H is the Hall coefficient, t is the thickness of the transducer, I is the current intensity and B is the magnetic field perpendicular to the current flow vector.

Unfortunately, in the real life, Hall transducer output voltage is affected by several second order effects.

The most important one is given by the presence of a parasitic voltage, called the offset voltage, at the sensing terminal of the transducer when no magnetic field is present.

The offset voltage is generated by several phenomena, the most important being the piezoresistive effect. When the die is subjected to mechanical stress the resistivity of the material changes locally; this changes translates into a residual voltage at the sense contacts of the sensor. Basically, the Hall transducer can be

modeled as a Wheatstone bridge (see Fig. 1). Ideally, in the absence of the magnetic field the bridge is balanced and the output voltage is zero. Due to piezoresistive effect the bridge arms are not even, resulting in a nonzero output voltage.

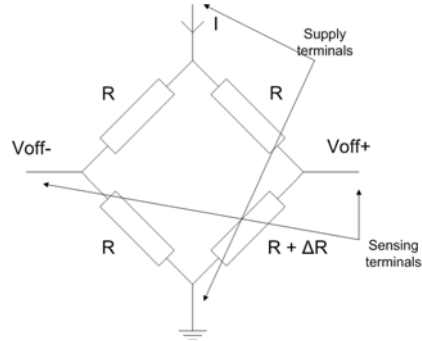


Fig. 1. Wheatstone bridge model for the offset voltage

Offset at the output of the Hall plates can also be generated by lithographic misalignment and etching randomness. These will not be treated separately, but will all be included in the general task of offset reduction.

3. Offset reduction using parallel connected transducers

Continuous time sensors are the most basic of the Hall effect sensors. Their architecture contains just a voltage regulator, the Hall transducer, an amplifier and a comparator with an output stage.

This minimal architecture drastically limits for possibilities of offset compensation. The most widely technique used in these types of sensors is the usage of several Hall transducers, connected in parallel, but having a different orientation on the silicon die. This compensates the offset of one Hall plate with the offset from another.

The major disadvantage of this technique is that the averaged offsets come from different Hall plates, and thus, will most likely have different values depending on the position of each transducer. However, for cheap sensors, with limited die area or systems very sensitive to noise or charge injection, this is the solution of choice.

The layout of the Hall transducers is very important in order to minimize the offset using this technique. For switch-type sensors, the transducers will be placed in the center of the silicon die, arranged so that they form a square. For differential-type sensors, the transducers will be placed in the middle of opposing sides of the die, either in a square or in a row.

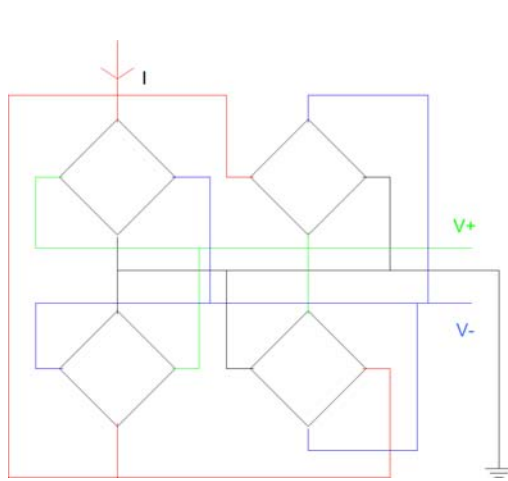


Fig. 2. Parallel Hall plate connection.

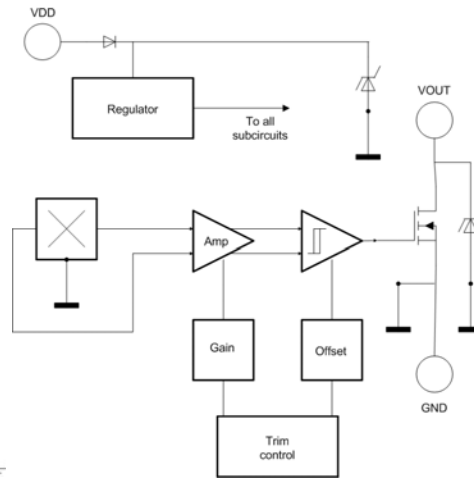


Fig. 3. Typical implementation of a continuous-time Hall effect sensor (Allegro Microsystems A1202)

Another disadvantage is that there is no improvement in the reduction of the amplifier offset. The output signal from a Hall plate biased hundreds of microamps, in magnetic fields under 10 mT is under 1 mV. This is smaller than the input offset of a differential CMOS input stage. That is why, for continuous time Hall sensors, a bipolar input stage for the amplifier is used when available, due to the much smaller offset we can obtain.

4. Offset reduction using spinning currents

Since the performance of continuous time sensors does not always satisfy the application needs, other techniques have been developed in order to reduce the effect of the offset voltage on the behavior of the sensor.

One of these techniques is the spinning currents technique. The basis is that current is injected through all the terminals of the Hall transducer, alternatively. After each injection step, the output voltage is memorized on capacitors, whose values are averaged after the spinning cycle has completed.

The spinning cycle can have two or four stage, depending on both required time-response and accuracy of the application. A two step spinning cycle will offer more speed, but smaller accuracy, while a four step spinning cycle will offer better accuracy, but slower speed.

It is important to note that the complexity of a sensor which uses current spinning is much greater than the one of continuous time sensors. This is due to the fact that several additional blocks are required, such as an oscillator, a sequencer, transfer gates and a capacitor bank for averaging.

To get a measure of the improvements brought by the spinning current technique, a comparison of two Hall effect switches, one with and one without this technique is done [8].

Table 1

| Performance comparison between different types of Hall switches | | | | |
|---|---------------------------|-----------|------------|------------|
| Sensor | Target positive threshold | Low limit | High limit | Tolerance |
| TLE4935G no spinning | not given | 10 mT | 20 mT | $\pm 50\%$ |
| TLE4946K with spinning and chopping | 14 mT | 11 mT | 17 mT | $\pm 20\%$ |

One can see the major improvement in tolerance for the magnetic threshold using the spinning current and amplifier chopping technique.

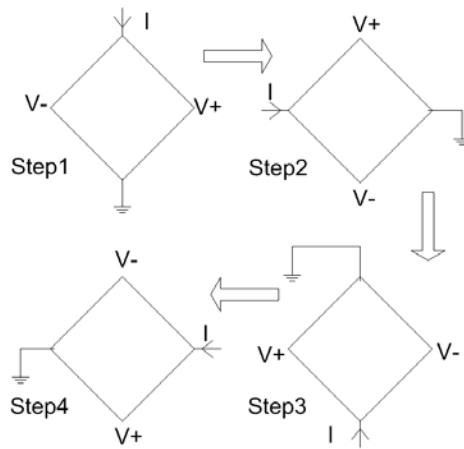


Fig. 4. Four step Hall plate spinning.

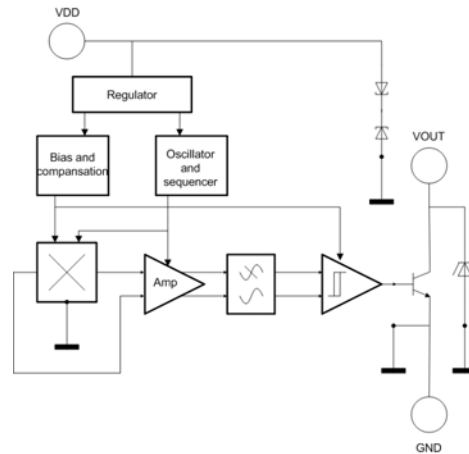


Fig. 5. Typical implementation of a chopper stabilized Hall effect sensor (Infineon - TLE4906)

5. Amplifier offset reduction

Since the signal generated by the Hall transducer for usual magnetic fields values (1...20 mT) is smaller than 1 mV, an amplifier with very low offset is required. This can be done using several methods.

The first one is based on bipolar input stage. Bipolar differential stages have lower offset voltages than their CMOS counterparts. Unfortunately, this requires the availability of a bipolar or BiCMOS process. While bipolar processes are cheap and very stable, they do not offer a compact layout, which makes the

resulting sensors large and package-costly. On the other hand, BiCMOS technologies offer the compactness of a CMOS technology and the availability of small digital logic, but are much more expensive, due to the additional masks and fabrication steps.

When good quality bipolar transistors are not available, as in standard CMOS processes, the offset of the input stage can be minimized by increasing the width and length of the transistors which are used in the input stage. However, in order to achieve the same offset performance as the bipolar input stage, the devices become too large to be practically implemented. That is why a pure CMOS sensor will have poorer offset performance than a bipolar one.

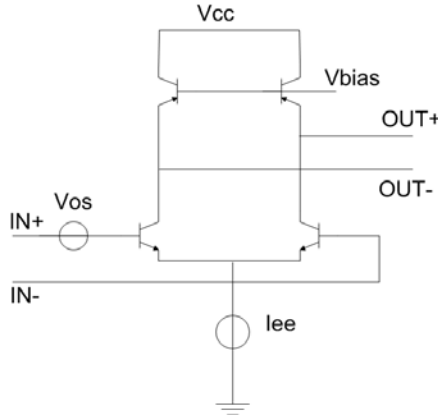


Fig.4. Bipolar input stage

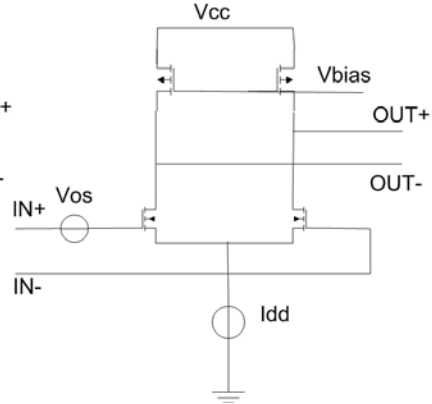


Fig.5. MOS input stage

The equivalent input offsets of the bipolar and MOS differential stages are given by:

$$V_{OS_bip} = V_T \left(-\frac{\Delta I_{S,pnp}}{I_{S,pnp}} - \frac{\Delta I_{S,npn}}{I_{S,npn}} \right) \quad 2)$$

respectively

$$V_{OS_MOS} = \Delta V_{th0,n} + \Delta V_{th0,p} \sqrt{\frac{\beta_p}{\beta_n}} + \frac{V_{GS} - V_{th0,n}}{2} \left(\frac{\Delta \beta_n}{\beta_n} + \frac{\Delta \beta_p}{\beta_p} \right) \quad 3)$$

where:

$$\beta_n = \mu_n C_{ox,n} \left(\frac{W}{L} \right)_n \quad 4)$$

$$\beta_p = \mu_p C_{ox,p} \left(\frac{W}{L} \right)_p \quad 5)$$

A third option to obtain amplifiers with very low offset is to use a chopper stabilized amplifier. This type of amplifier modulates the input offset at a high frequency and then removes it using a low-pass filter. To design such an amplifier, an additional amplifier and sequencer, as well as switches and a filter are required. But generally, the advantages outweigh the extra requirements in complexity and area, and most Hall effect switches employ this technique. The usage of a chopped amplifier does not pose bandwidth challenges, since the magnetic field frequency is smaller than 25 kHz, much lower than what regular integrated oscillators can achieve. To have a means of comparison, the typical input offset of a bipolar input stage is 0.1...2 mV, while for a MOS stage is in the order of 1...20 mV, [7]. This offset is reduced using chopping techniques to values of less than 100 μ V, [6].

Although chopping can reduce the input offset of the amplifier, integrating it into the signal path can prove difficult, since it has to be synchronized with the current spinning technique used for the Hall plates. Most of the times, this means that the chopping will be done at low frequencies, closer to the maximum frequency of the input signal. This in turn will result in large residual offset, since building a sharp filter requires a lot of silicon area and can cause different delays on the signal path, which will be frequency dependent.

5. Switched capacitor amplifiers

That is why we propose a new type of amplifier for the signal path. This will have a switched capacitor architecture, which brings a number of different advantages.

The first one and most important is that the offset can be removed altogether during the signal evaluation period, using correlated double sampling, which is very useful, and can bring large performance improvements.

Second, the overall static current consumption will be reduced, due to the fact that the feedback network is purely capacitive.

Third, the integration into the spinning current is very easy, and can be done with complicated clocking techniques.

However, there are several drawbacks. The first is that the signal path becomes time-discrete right from the beginning, but if the sampling frequency is high enough, there will be no performance loss. Second, the gain of the amplifier is limited by the ratio to which capacitors can be matched, by parasitic effects and by area consumption. This means that the comparator at the output stage needs to have a smaller offset than before.

But so far, the advantages seem to outweigh the drawbacks, and an implementation will be described in the following.

6. Switched capacitor feedback amplifier for Hall effect sensors

The core of the amplifier is a transconductance amplifier, with a PMOS input stage. This type of stage is required due to the common mode of the magnetic signal, which is closer to ground than to the supply rail. The input stage is followed by a folded cascode with differential output. Naturally, this requires a common mode feedback, which is integrated into upper current mirror. This type of amplifier can reach open-loop gain of over 80 dB and bandwidths over 10 MHz, which is more than enough for our needs.

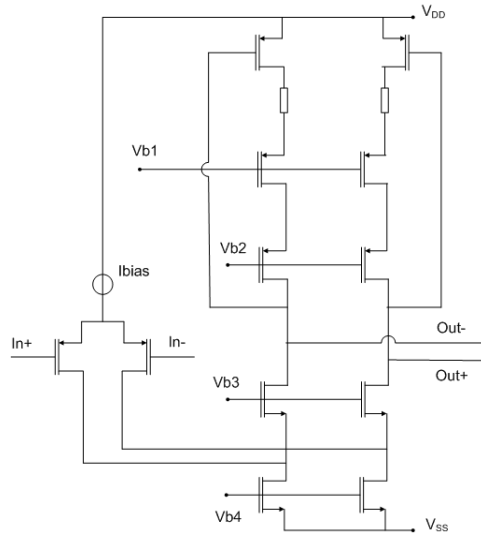


Fig. 5. Fully differential OTA

This amplifier will be used in a switched capacitor feedback loop, which is presented in the following figure. Besides the feedback loop, then outputs of the amplifier are connected to two voltage buffers, which store the amplifier outputs to the spinning current demodulation capacitors. The offset of the voltage buffers is not critical, since the differential signal has already been amplified.

Some design issues have to be taken into consideration. The switches should be designed as transfer gates, since the common mode of the input signal can have large variations depending on temperature and biasing. The capacitors on the feedback loop should be made of unit capacitor, positioned in a common centroid layout, to minimize mismatches. Also, the transfer gates should be matched in order to have symmetrical charge injection during the switching phases. Under ideal conditions, the amplification is given, [9], as:

$$V_{Od} = \frac{C_1}{C_2} V_{Id} \quad 6)$$

and the input referred offset is null. A thorough discussion related to the signal evaluation in switched capacitor amplifiers can be found in [9].

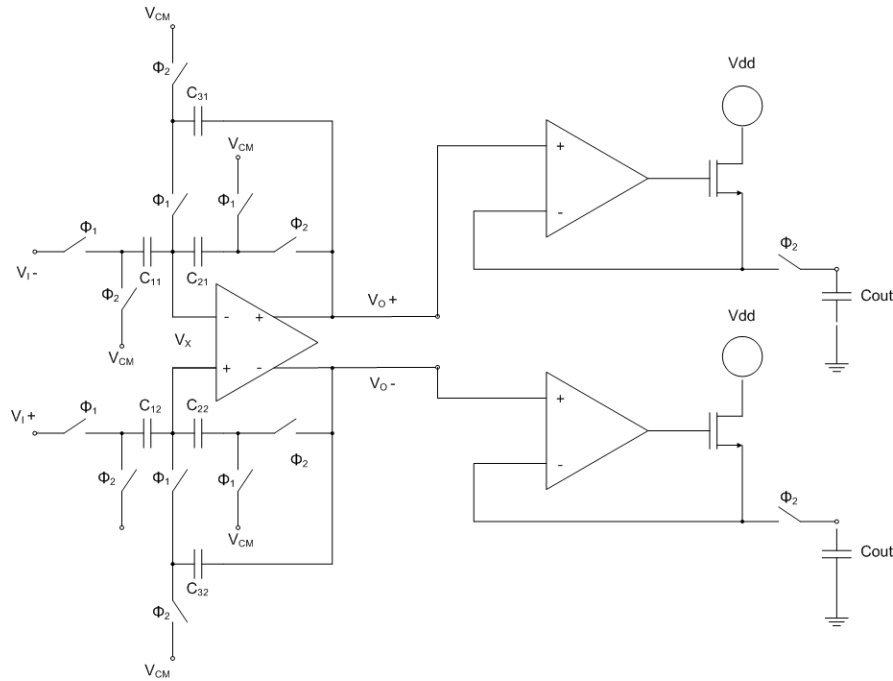


Fig. 6. Switched capacitor signal path for integrated Hall effect sensors

7. Conclusions

In the preceding discussions, we have presented a short overview of the system architectures used in the development of integrated Hall effect sensors.

Taking into consideration the previous aspects, we can now choose the right architecture for the sensor required in the application.

For cheap application, which do not require precision, multiple Hall transducers (usually four) connected in parallel and a bipolar input stage for the amplifier are the best option. These will provide adequate performance with low manufacturing and operation costs. If bipolar transistors are not available, then large CMOS transistors can be used instead, but with poorer performance parameters.

If higher accuracy is required, then the spinning currents method for the Hall transducers is used. This will provide much lower residual offsets. Since this method already requires an oscillator and a sequencer, it is usually combined with a chopping technique for the amplifier.

Since a four steps spinning cycle might be too slow for the application requirements, a compromise can be reached by using two parallel Hall plates onto which a two step spinning cycle is used. This will provide both passive (from the parallel connected Hall plates) and active (from the current spinning technique) offset reduction, and will also allow the use of a chopped amplifier.

In low noise applications, where the noise generated by the chopper is intolerable, one has to revert to the four-piece parallel layout for transducer offset reduction and the use of a bipolar stage for the amplifier.

Also, we have presented new amplifier architecture for the signal path of high precision switches. This uses a switched capacitor feedback, which brings many benefits, including smaller area footprint, lower current consumption and better offset rejection.

This amplifier can easily be integrated into the signal path of a spinning current biased Hall transducer, since it requires only two small buffers to supply the demodulation capacitors.

Using this architecture, better performance can be achieved for the Hall effect sensors.

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